RISC-V Core

Core Load/Store Unit

Accelerator Load/Store Unit

Hardware Memory Prefetcher

• • •

Arbiter

0   1   2   • • •   N-1

HPDcache

up to 64 bytes/cycle

HPDcache Core

1 request/ cycle

Data/Directory   CSRs

RTAB   MSHR   Write Buffer

Memory Interface   *up to 64 bytes/channel/cycle*

Read Request   Write/AMO Request